CMOS Analog Circuit Design

**Assignment – 1 ( PART -2)**

Q.1 Calculate the small-signal voltage gain of the CS stage shown below if *ID* = 1 mA, *μnCox* = 100 *μ*A*/*V2, *VTH* = 0*.*5 V, and *λ* = 0, *W/L* = 10*/*0*.*18 , Verify that *M*1 operates in saturation.



Q.2 Draw the circuit diagram of common source single stage amplifier with i) diode connected load with NMOS devices and ii) Resistive load. Compare the small signal voltage gains AV and comment on output impedance and output voltage swings of these two Amplifiers.

Q.3 Prove that the output is a linear function of input voltage in the case of a CS stage with source degeneration.

Q.4 In the common-source stage shown below *W/L* = 30*/*0*.*18 and *λ* = 0. (a) What gate voltage yields a drain current of 0.5 mA? (Verify that *M*1 operates in saturation.)Assume *μnCox* = 200 *μ*A*/*V2, *VTH* = 0*.*4 V



Q.5 In the circuit shown below, (*W/L*)1 = 10*/*0*.*18 and *ID*1 = 0*.*5 mA.(a) If *λ* = 0, determine (*W/L*)2 such that*M*1 operates at the edge of saturation.(b) Now calculate the voltage gain. (c) Explain why this choice of (*W/L*)2 yields the maximum gain. Assume *μnCox* = 200 *μ*A*/*V2, *VTH* = 0*.*4 V



Q.6 The common-gate stage shown below must provide a voltage gain of 4 and an input impedance of 50 ohms . If *ID* = 0*.*5 mA, and *λ* = 0, determine the values of *RD* and *W/L*. b) Suppose in Fig. 7.68, *ID* = 0*.*5 mA, *λ* = 0, and *Vb* = 1 V. Determine the values of*W/L* and *RD* for an input impedance of 50 *\_* and maximum voltage gain (while *M*1 remains in saturation). . Assume *μnCox* = 200 *μ*A*/*V2



Q.7 Using small signal model taking body effect into account , derive an expression for the voltage gain of a source follower and also plot the variation of voltage gain versus input voltage.

Q8. Explain the operation of cascode stage with allowable voltage sings and input-output characteristics.